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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/998,303 | 12/03/2001 | Sung-Chan Park | 08244.0032 | 4821 |

7590 03/31/2005

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| EXAMINER | |
|---|---|
| NGUYEN, THANH T | |
| **ART UNIT** | **PAPER NUMBER** |
| 2813 | |

DATE MAILED: 03/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/998,303 | PARK ET AL. | |
| | Examiner | Art Unit | |
| | Thanh T. Nguyen | 2813 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12/29/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Arguments*

Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim (U.S. Patent 5,318,925).

Referring to figures 4a-4d, Kim teaches a method for forming contact openings between bit line patterns, the method comprising the steps of:

a) forming bit line patterns (5') on a substrate (1, see figure 4a);

b) forming an interlayer insulating film (4) over the substrate;

c) etching the interlayer insulating film (4) by using the bit line patterns (5') and an etching mask (8) defining a straight line shape as a mask, thereby forming at least one straight line shaped self-aligned contact opening between neighboring bit line patterns (5', see figure 4a-4b); and

d) forming spacers (17) on the sidewalls of the bit line patterns only exposed through the contact opening (see figure 4c).

Regarding to claim 3, the interlayer insulating layer (24/26, oxide layer, col. 5, lines 20-35).

Regarding to claim 6, the top surfaces of the bit line patterns are covers with a layer selected from the group consisting of an oxide layer (16, see col. 4, lines 21-26).

Claims 1-3, 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Kohyama et al. (U.S. Patent 6,551,894).

Referring to figures 11-14, Kohyama et al. teaches a method for forming contact openings between bit line patterns, the method comprising the steps of:

a) forming bit line patterns (105, see figure 5, 8b-7g) on a substrate (11, see figure 5, 8b-7g, col. 7, and lines 1-22);

b) forming an interlayer insulating film (22, bpsg, see figure 9a) over the substrate;

c) etching the interlayer insulating film (22) by using the bit line patterns (BL/105) and an etching mask (27, silicon nitride) defining a straight line shape as a mask, thereby forming at least one straight line shaped self-aligned contact opening between neighboring bit line patterns (col. 7, lines 1-22, figures 9b); and

d) forming spacers (31/31a) on the sidewalls of the bit line patterns only exposed through the contact opening (see figure 9c).

regarding to claims 2-3, the interlayer insulating film oxide has a dielectric constant less than 3.5 (BPSG is a doped oxide film which has the dielectric constant less than the oxide film 3.5)

Regarding to claim 6, the top surfaces of the bit line patterns are covers with a layer selected from the group consisting of an silicon nitride layer (27, col. 7, lines 1-8).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 4-6, 9 are stand rejected under 35 U.S.C. 103(a) as being unpatentable over Kohyama et al. (U.S. Patent 6,551,894) applied to claims 1-3, 6 above or Kim (U.S. Patent 5,318,925) applied to claims 1, 6 above in view of further in view of cooper et al. (U.S. Patent No. 5,219,793).

Referring to figures 11-14, Kohyama et al. teaches a method for forming contact openings between bit line patterns, the method comprising the steps of:

a) forming bit line patterns (105, see figure 5, 8b-7g) on a substrate (11, see figure 5, 8b-7g, col. 7, and lines 1-22);

b) forming an interlayer insulating film (22, bpsg, see figure 9a) over the substrate;

c) etching the interlayer insulating film (22) by using the bit line patterns (BL/105) and an etching mask (27, silicon nitride) defining a straight line shape as a mask, thereby forming at least one straight line shaped self-aligned contact opening between neighboring bit line patterns (col. 7, lines 1-22, figures 9b); and

d) forming spacers (31/31a) on the sidewalls of the bit line patterns only exposed through the contact opening (see figure 9c).

regarding to claims 2-3, the interlayer insulating film oxide has a dielectric constant less than 3.5 (BPSG is a doped oxide film which has the dielectric constant less than the oxide film 3.5)

Regarding to claim 6, the top surfaces of the bit line patterns are covers with a layer selected from the group consisting of an silicon nitride layer (27, col. 7, lines 1-8).

However, none of the reference teach the interlayer insulating layer has a low dielectric constant is etched a gas mixture of $CF_4$, $CHF_3$, and argon (Ar) or using a gas selected from Ar, $O_2$, $N_2$, $H_2$, $CH_4$, $C_2H_4$ and $C_xF_y$ as claimed in claims 2-4, 8. Nevertheless, such processing step is known in the semiconductor processing art as evidenced by Cooper et al.. Cooper teaches forming an oxide interlayer insulating layer (18) and SOG layer (22, spin on glass, Noted SOG layer is a low dielectric oxide layer which has the dielectric constant less than 3.5 as claimed in claims 2-3) is etched with a mixture of $CF_4$, $CHF_3$, and argon (Ar) or one of Ar, $O_2$ and $C_2F_6$, at the pressure of 150-350 mtorr (see col. 5, lines 4-19). It would have been obvious to a person of ordinary skill in the art at the time of the invention was made would have used a mixture of $CF_4$, $CHF_3$, and argon (Ar) or one of Ar, $O_2$ and $C_2F_6$ to etch the interlayer insulating layer in

Kohyama et al (or Kim)'s process as taught by Cooper et al. ***because*** carbon and fluorine compound plasma can selectively etch the oxide interlayer insulating layer and remove all the oxide interlayer layer to expose the contact region between conductive patterns, and in the case when some spacing between conductive patterns wider than the other, the carbon and fluorine compound plasma can selectively etch the oxide interlayer insulating layer and leave a portion of oxide interlayer insulating layer on the sidewall of the conductive patterns to form sidewall spacers and also expose the contact region between the conductive patterns.

Regarding to claim 6, method of forming a mask pattern covering a top portion of the conductive layer pattern wherein the mask pattern is formed of a layer selected from a group consisting of silicon nitride. Nevertheless, such processing step is known in the semiconductor processing art as evidenced by Cooper. Cooper teaches forming a mask pattern (16) covering a top portion of the conductive layer pattern (14) wherein the mask pattern (16) is formed of a layer selected from a group consisting of silicon nitride (see figure 1 and col. 3, lines 52-63). It would have been obvious to a person of ordinary skill in the art at the time of the invention was made would have formed a silicon nitride mask pattern covering a top portion of the conductive layer pattern in the Kohyama et al (or Kim)'s process as taught by Cooper et al. ***because*** the silicon nitride mask pattern provides protection to the top surface of conductive layer pattern during the etching process of interlayer insulating layer, so that the top surface of the conductive layer pattern can not be etched or damaged by the chemical or plasma.

Regarding to claims 5, 9, the specific etching pressure range as claimed are taken to be obvious since these are variables of art recognized importance which are subject to routine

experimentation and optimization and discovery of an optimum value for a known process is obvious. In re Aller, 105 USPQ 233 (CCPA 1955). And, even if applicants' modification results in great improvement and utility over the prior art, it may still not be patentable if the modification was within the capabilities of one skilled in the art, In Re Sola 25 USPQ 433. Since, Cooper teaches that the oxide interlayer insulating layer (18, 22) is etched with a mixture of $CF_4$, $CHF_3$, and argon (Ar) or one of Ar, $O_2$ and $C_2F_6$ at the pressure of 150-350 mtorr (see col. 5, lines 4-19), hence, one of ordinary skill in the requisite art at the time the invention was made would have adjusted the plasma etching pressure to the range of less than 100 mtorr to etch the interlayer insulating layer ***because*** when an optimum etching pressure in the etching chamber is used to etch the interlayer insulating layer, the interlayer insulating layer in the contact region can be completely removed or at the same time leaving a portion of the interlayer insulating layer on the sidewall of conductive layer patterns depending on the spacing between the conductive layer patterns.

Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kohyama et al. (U.S. Patent 6,551,894) applied to claims 1-3, 6 above or Kim (U.S. Patent 5,318,925) applied to claims 1, 6 above in view of further in view of Chang et al. (U.S. Patent No. 6,159,842) and further in view of Tsai et al. (U.S. Patent No. 6,331,480).

Regarding to claim 7, the interlayer insulating layer is formed of a polymer. Nevertheless, such processing step is known in the semiconductor processing art as evidenced by Chang et al. Chang et al. teaches forming a low dielectric constant material layer HSQ layer (18) having a dielectric constant about 3 over the conductive layer patterns (14) (see figure 1 and col.

4, lines 22-40). The HSQ layer is a silicon polymer and spin-on insulating oxide material having a dielectric constant of 2.7-3.0 (see col. 1, lines 50-55). It would have been obvious to a person of ordinary skill in the art at the time of the invention was made would have used a silicon polymer HSQ layer having low dielectric constant to replace Kohyama et al (or Kim)'s low dielectric interlayer insulating layer as taught by Chang et al. ***because*** silicon polymer HSQ layer can be easily deposited over the conductive layer patterns by spin-on coating process, and HSQ material also has the same low dielectric constant characteristics as the other low dielectric constant material which eliminates the capacitive interaction or coupling between closely-spaced conductive layer patterns.

Regarding to claim 8, the interlayer insulating layer is formed of a polymer and etched with a gas selected from Ar, $O_2$, $N_2$, $H_2$, $CH_4$, $C_2H_4$ and $C_xF_y$. Nevertheless, such processing step is known in the semiconductor processing art as evidenced by Tsai et al. Tsai et al. teaches etching low dielectric constant material HSQ having a dielectric constant of about 2.5-3.5 with an etchant of $O_2/C_2F_6$ (see col. 3, lines 15-21).

Since, Chang et al. teaches forming a low dielectric constant material layer of polymer HSQ layer over the conductive layer patterns having a dielectric constant of 2.7-3.0. It would have been obvious to a person of ordinary skill in the art at the time of the invention was made would have etched a silicon polymer HSQ layer with an etchant of $O_2/C_2F_6$ in Chang et al.'s process as taught by Tsai et al. ***because*** Chang et al. and Tsai et al. both have similar HSQ material, and HSQ material layer which can be selectively etched with $O_2$ and/or $C_2F_6$ to form spacers on the sidewall of conductive layer pattern and/or expose the conductive region.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (703) 308-9439, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, can be reached on (703) 308-4940. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956 (**See MPEP 203.08**).

Thanh Nguyen
Patent Examiner
Patent Examining Group 2800

TTN